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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,326	12/01/2003	Fwu-Iuan Hshieh	GS 145 D1	2693
27774	7590	07/26/2004	EXAMINER	
MAYER, FORTKORT & WILLIAMS, PC 251 NORTH AVENUE WEST 2ND FLOOR WESTFIELD, NJ 07090			CAO, PHAT X	
		ART UNIT	PAPER NUMBER	
			2814	

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/725,326	HSHIEH ET AL.
	Examiner	Art Unit
	Phat X. Cao	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 01 December 2003.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 24-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 24-30 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

- Certified copies of the priority documents have been received.
- Certified copies of the priority documents have been received in Application No. _____.
- Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 12/1/03.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____.

DETAILED ACTION

1. The cancellation of claims 1-23 in Paper filed 12/01/03 (Preliminary Amendment) is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 24-25 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Okabe et al (US. 5,925,911).

Regarding claim 24, Okabe (Figs. 3-10) discloses a method of forming a trench DMOS transistor device comprising: providing a substrate 1 of a first conductivity type (N+), the substrate acting as a common drain region for the device (column 4, lines 3-4); depositing an epitaxial layer 2 of the first conductivity type (N-) over the substrate, the epitaxial layer 2 (N-) having a lower majority carrier concentration than the substrate 1 (N+); forming a body region 40 of a second conductivity type (P) within an upper portion of the epitaxial layer 2; etching a trench 60 extending into the epitaxial layer 2 from an upper surface of the epitaxial layer 2 (Fig. 7); forming an insulating layer 6 lining at least a portion of the trench (see Fig. 10 and column 5, lines 55-60); forming a conductive region 7 within the trench adjacent the insulating layer; forming a source region 5 of the first conductivity type (N+) within an upper portion of the body region 40 and adjacent the trench; and forming a low resistivity deep region 31 of N+ extending into the device

from an upper surface of the epitaxial layer 2, the deep region 2 acting to provide electrical contact with the substrate 1.

Regarding claims 25 and 28, Okabe's Fig. 10 further discloses: the deep region 31 comprising a semiconductor region of the first conductivity type (N+) that is formed by an implantation and diffusion process (column 5, lines 14-18); a metallic drain contact 14 adjacent an upper surface of the deep region 31, a metallic source contact 9 adjacent an upper surface of the source region (corresponding to "SECOND REGION" of Fig. 10), and a metallic gate contact (not labeled) adjacent an upper surface of the conductive region in a termination region (corresponding to "FIRST REGION" of Fig. 10) remote from the source region (SECOND REGION).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 24 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Darwish et al (US. 5,674,766).

Regarding claim 24, Darwish (Fig. 3D) discloses a method of forming a conventional trench DMOS transistor device comprising: providing a substrate 120 of a first conductivity type (N=), the substrate 120 acting as a common drain region for the device; depositing an epitaxial layer 111 of the first conductivity type (N) over the substrate 120, the epitaxial layer 111 having a low majority carrier concentration than

the substrate 120; forming a body region 114 of a second conductivity type within an upper surface of the epitaxial layer 111; etching a trench extending into the epitaxial layer 111 from an upper surface of the epitaxial layer 111; forming an insulating layer (not labeled) lining at least a portion of the trench; forming a conductive region 102 within the trench adjacent the insulating layer; and forming a source region (not labeled) of the first conductivity type (N+) within an upper portion of the body region 114 and adjacent the trench.

Darwish's Fig. 3D does not disclose a low resistivity deep region extending from an upper surface of the epitaxial layer 111 to the substrate 120. However, Darwish's Fig. 13 teaches the forming of a low resistivity deep region 304 of N+ type extending from an upper surface of the epitaxial layer to the substrate 318. Accordingly, it would have been obvious to include in Darwish's Fig. 3D a low resistivity deep region with the structure as set forth in Darwish's Fig. 13 because such forming of the low resistivity deep region would provide an electrical contact to the drain or the substrate 318 (column 11, lines 15-19).

Regarding claim 28, Darwish further discloses: a metallic drain contact 306 (Fig. 13) adjacent an upper surface of the deep region 304, a metallic source contact 118 (Fig. 3D) adjacent an upper surface of the source region, and a metallic gate contact 121 (Fig. 3D) adjacent an upper surface of the conductive region in a termination region remote from the source region.

6. Claims 26-27 and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okabe et al or Darwish et al in view of Kubo (US. 5,463,241).

Regarding claims 26-27, neither Okabe nor Darwish disclose the deep region formed by a method as claimed.

However, Kubo (Figs. 6B-6D) teaches the forming a deep region 101 comprising a low resistivity material such as doped polycrystalline silicon and refractory metals (column 4, lines 56-59), wherein the deep region 101 is formed by a process comprising etching a deep trench 200 (Fig. 6B) that extends into the device from an upper surface of the epitaxial layer 1b (P-) and depositing doped polycrystalline silicon or refractory metals 101 within the deep trench 200. Accordingly, it would have been obvious to modify the process of Okabe and Darwish by forming the deep region with the process as set forth above, because as taught by Kubo, such modified process would form the deep region with the low resistivity materials for reducing source/drain resistance, improving high frequency gains and improving heat dissipation characteristics (column 5, lines 45-55).

Regarding claims 29-30, Kubo further discloses the low resistivity deep region 101 extending from the upper surface of the epitaxial layer 1b to the substrate 1a, and having a resistivity in a range as claimed because the deep region 101 is made by refractory metal which has a low resistivity (column 4, lines 56-59).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
July 23, 2004

Caomhanh
PHAT X. CAO
PRIMARY EXAMINER